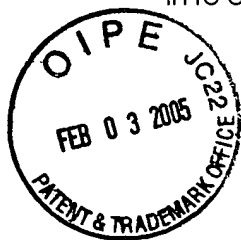


IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:



WARREN M. FARNWORTH
ALAN G. WOOD
WILLIAM M. HIATT
JAMES M. WARK
DAVID R. HEMBREE
KYLE K. KIRBY
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EXAMINER:

Serial No.: 10/730,333

ART UNIT:

Filing Date: 12/08/2003

FOR: WAFER LEVEL METHODS FOR FABRICATING
MULTI-DICE CHIP SCALE SEMICONDUCTOR
COMPONENTS (AS AMENDED)

Docket No. 02-1500.1

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.56

JANUARY 31, 2005

Mail Stop Amendment
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

The citations listed on the accompanying Form PTO/SB/08, may be material to the examination of the subject application and are therefore submitted in compliance with the duty of disclosure defined in 37 CFR §§1.56, 1.97 and 1.98.

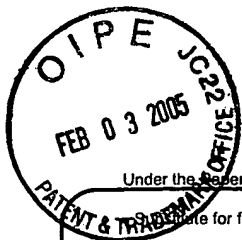
This Information Disclosure Statement under 37 CFR §§1.56, 1.97 and 1.98 is not to be construed as a representation that a search has been made, that additional material to the examination of this application does not exist, or that any one or more of these citations constitutes prior art under 35 USC §102.

It is requested that the above citations be made of record, if appropriate, in the prosecution of this application.

Respectfully submitted:

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PTO/SB/08A (08-03)

Approved for use through 07/31/2006. OMB 0651-0031

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9-889-01-001-0001
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STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number	10/730,333
Filing Date	12/08/2003
First Named Inventor	WARREN M. FARNWORTH
Art Unit	
Examiner Name	
Attorney Docket Number	02-1500.1

Sheet 1 of 1

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	A	US- 6,841,883 B1	01/11/2005	Farnworth et al.	
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FOREIGN PATENT DOCUMENTS

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